ABSTRACT OF THE DISCLOSURE

A computer system includes a plurality of memory modules that contain semiconductor memory, such as DIMMs. The system includes a host/data controller that utilizes an XOR engine to store data and parity information in a striped fashion on the plurality of memory modules to create a redundant array of industry standard DIMMs (RAID). The host/data controller also interleaves data on a plurality of channels associated with each of the plurality of memory modules. To optimize memory bandwidth and reduce memory latency, various techniques are implemented in the present RAID system. Present techniques include providing dual memory arbiters, sorting read cycles by chip select or bank address, providing programmable upper and lower boundary registers to facilitate programmable memory mapping, and striping and interleaving memory data to provide a burst length of one.